Amendments to the Claims

This listing of claims will replace all prior versions, and listing, of claims in the application:

1. (Currently Amended) An integrated circuit arrangement on the basis of III/V semiconductors, comprising at least one active component (2) and a multilayer configuration of wiring levels, characterized in that:

a metallization layer comprising a metal contact (4) of the at least one active component (2) is formed to be a lower one of the wiring levels, and that

said lower one of the wiring levels is deposited directly on top of a subcollector layer without a passivation layer (8) underneath the lower wiring level, and connects the at least one active component with at least one passive component.

2. (Currently Amended) The integrated circuit arrangement as claimed in claim 1, characterized in that a the passivation layer (8) is made of a material which has a small relative dielectric constant εr1 that obeys the equation [[(]]εr1<3[[)]], and is applied on the metallization layer of the at least one active component (2).

3. (Currently Amended) The integrated circuit arrangement as claimed in claim 1, characterized in that:

an electric resistor is formed in the lower wiring level (30) by means of an interruption (7) in the metallization layer, and that

no additional resistive material is placed in the interruption in the metallization layer.

4. (Currently Amended) The integrated circuit arrangement as claimed in claim 2, characterized in that:

a central wiring level (11) is disposed above the passivation layer (8) and is covered by another passivation layer (13) made of a material which has a mean relative dielectric constant εr2 that obeys the equation [[()]εr2>εr1[()].

5. (Original) The integrated circuit arrangement as claimed in claim 4, characterized in that an upper wiring level (14) is disposed above the central passivation layer.

6. (Original) The integrated circuit arrangement as claimed in claim 4, characterized in that a capacitive component is formed by means of a section (17) of the central wiring level (11) and a section (18) of the upper wiring level (14).

7. (Original) The integrated circuit arrangement as claimed in claim 6, characterized in that the upper wiring level (14) is formed by galvanic deposition of metal.

8. (Previously Presented) The integrated circuit arrangement as claimed in claim 6, characterized in that the upper wiring level (14) is constructed at least partly by air bridge technology.

9. (Currently Amended) The integrated circuit arrangement as claimed in claim 1, characterized in that:

the at least one active semiconductor component (2) is a transistor; and

a metal contact (4) of the collector of the transistor is formed by means of the metallization layer.

10. (Previously Presented) The integrated circuit arrangement as claimed in claim 5, characterized in that at least one microstrip conductor is formed by means of the lower, the central, and the upper wiring levels (30, 11, 14).

11. (Previously Presented) The integrated circuit arrangement as claimed in claim 5, characterized in that waveguides are formed on the lower and/or the central and/or the upper wiring levels (30, 11, 14).

12. (Currently Amended) The integrated circuit arrangement as in claim 4, wherein the mean relative dielectric constant obeys the equation $\varepsilon r2$ ~~is~~ ≈ 7.